ABSTRACT OF THE DISCLOSURE

A circuit and method is provided for determining the delay of an integrated circuit common associated with chip-to-chip variations in the manufacturing process, changes in operating voltage, and fluctuations in temperature. A clock signal is inverted, thus generating an inverted clock signal which is then delayed multiple times, resulting in several delayed versions of the inverted clock signal, with each version being delayed a different length of time. The logical state of each delayed version of the inverted clock signal is then stored. That stored logical state provides an indication as to the magnitude of the delay of the integrated circuit which may then be used to tune critical signals of the integrated circuit to avoid timing problems resulting from variations in IC propagation delay.